Printed page: 02…. **Subject Code: AMTVL0101**

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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M. Tech

(SEM: I THEORY EXAMINATION (2020-2021)

Subject Name: CMOS Digital VLSI Design

Time: 3 Hours **Max. Marks:70**

General Instructions:

- All questions are compulsory. Answers should be brief and to the point.
- This Question paper consists of 02 pages & 08 questions.
- It comprises of three Sections, A, B, and C. You are to attempt all the sections.
- Section A -Question No- 1 is objective type questions carrying 1 mark each, Question No- 2 is very short answer type carrying 2 mark each. You are expected to answer them as directed.
- Section B - Question No-3 is Long answer type -I questions with external choice carrying 4marks each. You need to attempt any five out of seven questions given.
- Section C -Question No. 4-8 are Long answer type –II (within unit choice) questions carrying 7marks each. You need to attempt any one part *a* or *b.*
- Students are instructed to cross the blank sheets before handing over the answer sheet to the invigilator.
- No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION – A

1. Answer all the parts **[5x1=5]** **CO**

a. The device that is normally cut-off with zero gate bias is _____ mode transistor **(1)** **CO 1**

a. Enhancement
b. Depletion
c. nMOS
d. pMOS

b. A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called _____device. **(1)** **CO 2**

a. pull down
b. pull up
c. co-axial
d. co-centric

c. The threshold voltage Vth is not constant w. r. to the voltage difference between the substrate and the source of MOS transistor. This effect is called _____ **(1)** **CO 3**

a. substrate-bias effect or body effect
b. threshold effect
c. mix effect
d. none of these

d. _____ is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between VDD and VSS with disastrous results. **(1)** **CO 4**

a. Latch up
b. Hold up
c. Trigger
d. Threshold

e. _____is the time taken for a waveform to rise from 10% to 90% of its steady-state value. **(1)** **CO 5**

a. Fall Time
b. Rise Time
c. Setup time
d. Delay Time

2. Answer all the parts- **[5×2=10]** **CO**

a.	Compare BJT and CMOS	**(2)**	**CO 1**
b.	What do you mean by Speed Power Product?	**(2)**	**CO 2**
c.	What is Euler's Graph?	**(2)**	**CO 3**
d.	What do you mean by Voltage Bootstrapping?	**(2)**	**CO 4**
e.	What is Flash Memory?	**(2)**	**CO 5**

SECTION – B

CO

3. Answer any five of the following- **[5x4=20]**

a.	Explain the characteristics of nMOS in detail.	**(4)**	**CO 1**
b.	Explain the working of nMOS in detail with regions of operation.	**(4)**	**CO 1**
c.	Explain various Semiconductor Memories.	**(4)**	**CO 5**
d.	What do you mean by PASS Transistor Logic? Explain it's usage.	**(4)**	**CO 4**
e.	Explain Domino Logic.	**(4)**	**CO 4**
f.	Comment on AOI and OIA gates with suitable example.	**(4)**	**CO 3**
g.	Explain Latch-up effect.	**(4)**	**CO 3**

SECTION – C

CO

4 Answer any one of the following- **[5×7=35]**

a.	Draw the schematic and layout of Y= A. (B+C) + D.E. Explain with Euler's graph.	**(7)**	**CO 3**
b.	With neat sketches, explain in detail, all the steps involved in IC Fabrication process.	**(7)**	**CO 1**

5. Answer any one of the following-

a.	Explain the concept of Noise Margin. Find out the noise margin for any one type of Inverter.	**(7)**	**CO 2**
b.	Explain Switching characteristics of MOSFETs alongwith Rise Time, Fall Time, Setup Time and Hold Time.	**(7)**	**CO 2**

6. Answer any one of the following-

a.	Explain Transmission Gates. Implement any one gate using Transmission Gates.	**(7)**	**CO 3**
b.	Explain the working of Resistive Load Inverter circuit with suitable regions of operation.	**(7)**	**CO 2**

7. Answer any one of the following-

a.	Derive an equation for I_{ds} of an n channel enhancement MOSFET operating in saturation region.	**(7)**	**CO 2**
b.	An n MOS transistor is operating in saturation region with the following parameters, Vgs=5V, V_{tn} =1.2V, (W/L) =10, $\mu_n c_{ox}$=110μA/V ^{2}. Find trans conductance of the device.	**(7)**	**CO 2**

8. Answer any one of the following-

a.	Calculate the rise time and fall time of the CMOS inverter with the following parameters: $(W/L)_n$= 6 and $(W/L)_p$=8, K'_n =150μA/V^2, V_{tn} =0.7V, K'_p= 62 μA/V^2, V_{tp}=-0.85V , V_{DD} =3.3V. Total output capacitance =150 pF.	**(7)**	**CO 2**
b.	Describe the NOR and NAND flash memory with neat diagram.	**(7)**	**CO 5**