Printed page: 02… **.Subject Code: AMTVL0102**

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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY , GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

MASTER OF TECHNOLOGY (M. Tech)

(SEM: First Theory Examination (2020-2021)

SUBJECT NAME: ADVANCED DIGITAL DESIGN USING VERILOG

Time: 3 Hours **Max. Marks:70**

General Instructions:

- All questions are compulsory. Answers should be brief and to the point.
- This Question paper consists of 02 pages & 08 questions.
- It comprises of three Sections, A, B, and C. You are to attempt all the sections.
- Section A -Question No- 1 is objective type questions carrying 1 mark each, Question No- 2 is very short answer type carrying 2 mark each. You are expected to answer them as directed.
- Section B - Question No-3 is Long answer type -I questions with external choice carrying 4marks each. You need to attempt any five out of seven questions given.
- Section C -Question No. 4-8 are Long answer type –II (within unit choice) questions carrying 7marks each. You need to attempt any one part *a* or *b*.
- Students are instructed to cross the blank sheets before handing over the answer sheet to the invigilator.
- No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION – A

1.	**Answer all the parts-**		**[5x1=5]**	**CO**
	a.	Who developed the Verilog? a) Moorby b) Thomas c) Russell and Ritchie d) Moorby and Thomson	**(1)**	**CO 1**
	b.	Each unit to be modelled in a Verilog design is known as a) behavioural model b) design architecture c) design entity d) all of the Above	**(1)**	**CO 2**
	c.	In a digital clock application, the basic frequency must be divided down as _____ a) 1 Hz b) 60 Hz c) 100 Hz d) 1000 Hz	**(1)**	**CO 3**
	d.	Data path: perform data-processing operations between _____ a) registers b) capacitor c) clocks d) switch	**(1)**	**CO 4**
	e.	A K-Stage Pipeline is an acyclic circuit having exactly K _____on every path from an input to an output. a) registers b) capacitor c) clocks d) switch	**(1)**	**CO 5**

2.	**Answer <u>all</u> the parts-**		**[5×2=10]**	**CO**
	a.	Which delay is called as simulation delay model ?	**(2)**	**CO 1**
	b.	Which type of delays are used in behavioural model code ?	**(2)**	**CO2**
	c.	Which technology is avoided by combinational logic ?	**(2)**	**CO 3**
	d.	What is Switch Level Modeling?	**(2)**	**CO 4**
	e.	What is the THROUGHPUT of a K-pipeline?	**(2)**	**CO 5**

SECTION – B

3.	**Answer any <u>five</u> of the following-**		**[5x4=20]**	**CO**
	a.	Which are the different types of Design Methodologies? Explain them with examples.	**(4)**	**CO 1**
	b.	What are the different types modelling styles used in Verilog language and explain any one modelling with example.	**(4)**	**CO 2**
	c.	Explain styles for synthesis of combinational logic.	**(4)**	**CO 3**
	d.	Explain switch level modelling.	**(4)**	**CO 4**
	e.	Explain Pipelining Methodology.	**(4)**	**CO 5**
	f.	Explain different types of data path operators ?	**(4)**	**CO 4**
	g.	Write a Verilog program for full adder circuit?	**(4)**	**CO 2**

SECTION – C

4	**Answer any <u>one</u> of the following-**		**[5×7=35]**	**CO**
	a.	Explain Data types in Verilog with examples.	**(7)**	**CO 1**
	b.	Explain different types of operators used in Verilog language	**(7)**	**CO 1**
5.	**Answer any <u>one</u> of the following-**			
	a.	Draw the logical diagram of 4X1 Multiplexer. Write a Verilog program for 4X1 Multiplexer.	**(7)**	**CO 2**
	b.	Explain blocking & non-blocking assignments with example.	**(7)**	**CO 2**
6.	**Answer any <u>one</u> of the following-**			
	a.	Explain the concept of synthesis? Explain step by step process of synthesis.	**(7)**	**CO 3**
	b.	Write a short note on any one of the following- (i) Partitioning for synthesis. (ii) Optimization of Arithmetic Expression	**(7)**	**CO 3**
7.	**Answer any <u>one</u> of the following-**			
	a.	Explain the block diagram of Mealy and Moore state machine.	**(7)**	**CO 4**
	b.	Explain modelling register banks in details.	**(7)**	**CO 4**
8.	**Answer any <u>one</u> of the following-**			
	a.	Explain Pipeline Control Issues and Hardware	**(7)**	**CO 5**
	b.	Explain the concept of Basic pipelining	**(7)**	**CO 5**