Printed Page:- Subject Code:- AMTVL0102

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute)

Affiliated to Dr. A.P.J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow

M.Tech

SEM: I - THEORY EXAMINATION (2021 - 2022)

Subject: Advanced Digital Design using Verilog

Time: 03:00 Hours Max. Marks: 70

General Instructions:

1. All questions are compulsory. It comprises three Sections A, B and C.

- Section A - Question No- 1 is objective type question carrying 1 mark each & Question No- 2 is very short type questions carrying 2 marks each.
- Section B - Question No- 3 is Long answer type - I questions carrying 4 marks each.
- Section C - Question No- 4 to 8 are Long answer type - II questions carrying 7 marks each.
- No sheet should be left blank. Any written material after a Blank sheet will not be evaluated/checked.

SECTION A 15

1. Attempt all parts:-

1-a. When a key is pressed, what does the ring counter in the HDL keypad application do? (CO1) 1

1. Count to find the row
2. Freeze
3. Count to find the column
4. Start the D flip-flop

1-b. Cycle based simulation is useful for (CO2) 1

1. Synchronous circuit
2. Asynchronous circuit
3. Both
4. None

1-c. Which of the following can have more than one driver? (CO3) 1

1. IN
2. OUT
3. INOUT
4. BUFFER

1-d. In FSM diagram what does circle represent? (CO4) 1

1. Change of state
2. State
3. Output value
4. Initial state

1-e. Which of the architecture is power efficient? (CO5) 1

1. CISC
2. RISC
3. ISA
4. IANA

2. Attempt all parts:-

2-a. How we define vector data type. (CO1) 2

2-b.	Discuss behavioural and structural modeling with suitable examples. (CO2)	2
2-c.	Explain the term control and data flow graph(CDFG) (CO3)	2
2-d.	Draw the circuit diagram for an OR gate using nMOS and pMOS switches. (CO4)	2
2-e.	Give an example for case statement. (CO5)	2

SECTION B 20

3. Answer any five of the following:-

3-a.	Explain implicit continuous assignment delay in dataflow modeling. (CO1)	4
3-b.	Discuss different types of data path operators. (CO1)	4
3-c.	Write Verilog code for SR FF. (CO2)	4
3-d.	Write Verilog code for clock generation using always block. (CO2)	4
3-e.	Explain term end module in Verilog with example. (CO3)	4
3-f.	Explain Bit Slicing. (CO4)	4
3-g.	Write down the limitations of Pipelining. (CO5)	4

SECTION C 35

4. Answer any one of the following:-

4-a.	Differentiate between data flow and gate level modeling. (CO1)	7
4-b.	Differentiate between behavioural and structural modeling. (CO1)	7

5. Answer any one of the following:-

5-a.	Implement Full Subtractor circuit using gate level modeling. (CO2)	7
5-b.	Write Verilog code for clock generation using forever loop. (CO2)	7

6. Answer any one of the following:-

6-a.	Write a verilog code for priority encoder using Verilog and explain with a neat block diagram. (CO3)	7
6-b.	Write program for Moore machine in Behavioral models. (CO3)	7

7. Answer any one of the following:-

7-a.	Explain in detail about Finite State Machine. (CO4)	7
7-b.	Explain in detail about Modeling modules of Datapath. (CO4)	7

8. Answer any one of the following:-

8-a.	Write Verilog code for 4 bit SIPO shift register in Behavioral modeling. (CO5)	7
8-b.	With proper example explain how to initialize the memory using Verilog functions. (CO5)	7