Printed Page:- **Subject Code:- ACSE0304**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: III - CARRY OVER THEORY EXAMINATION - AUGUST 2023

Subject: Digital Logic & Circuit Design

Time: 3 Hours **Max. Marks: 100**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION A **20**

1. Attempt all parts:-

1-a. The logical expression Y = Σm(0, 3, 6, 7, 10, 12, 15) is equivalent to (CO1) 1

(a) πM(0, 3, 6, 7, 10, 12, 15)

(b) πM(1, 2, 4, 5, 8, 9, 11, 13, 14)

(c) Σm(1, 2, 4, 5, 8, 9, 11, 13, 14)

(d) Σm(0, 2, 4, 6, 8, 10, 12, 14)

1-b. There are _____ Minterms for 3 variables (a, b, c) (CO1) 1

(a) 12

(b) 10

(c) 4

(d) 8

1-c. There are _____ cells in a 4-variable K-map. (CO2) 1

(a) 16

(b) 12

(c) 18

(d) 8

1-d. What is the major difference between half-adders and full-adders? (CO2) 1

(a) Nothing basically; full-adders are made up of two half-adders

(b) Full adders can handle double-digit numbers.

(c) Full adders have a carry input capability.

(d) Half adders can handle only single-digit numbers.

1-e. A basic S-R flip-flop can be constructed by cross-coupling of which logic gates? (CO3) 1

(a) AND or OR gates

(b) XOR or XNOR gates

(c) NOR or NAND gates

(d) AND or NOR gates

1-f. The SR latch consists of (CO3) 1

(a) 2 inputs

(b) 1 input

(c) 3 inputs

(d) 4 inputs

1-g. Which of the following is an advantage of a synchronous reset? (CO4) 1

(a) It is slow

(b) It requires a clock signal to reset the circuit

(c) It filters the reset signal

(d) It needs a stretched reset

1-h. The table that is not a part of the asynchronous analysis procedure is (CO4) 1

(a) ExcitationTable

(b) Transition Table

(c) State Table

(d) Flow Table

1-i. The difference between a PAL & a PLA is _____ (CO5) 1

(a) PALs and PLAs are the same thing

(b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane

(c) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane

(d) The PAL has more possible product terms than the PLA

1-j. The communication between memory and its environment is achieved through _____. (CO5) 1

(a) Control lines

(b) Data input/output lines

(c) Address selection lines

(d) All of the Mentioned

2. Attempt all parts:-

2.a. Draw the logical circuit of AND Gate using NAND Gate. (CO1) 2

2.b. Define encoder. (CO2) 2

2.c. Define binary counter. (CO3) 2

2.d. Define synchronous and asynchronous circuits. (CO4) 2

2.e. Why are ROMs called non-volatile memory? (CO5) 2

SECTION B **30**

3. Answer any <u>five</u> of the following:-

3-a. Construct the Hamming code for the 4 bit data 1010. Consider the even parity. (CO1) 6

3-b. Minimize the given Boolean Expression by using the four-variable K-Map. 6
F (A, B, C, D) = Σ m (1, 5, 6, 12, 13, 14) + d (2, 4). (CO1)

3-c. Design a 16-to-1 multiplexer using two 8-to-1 multiplexer having an active-LOW Enable input. (CO2) 6

3-d. Implement the SUM and CARRY Boolean functions of full adder using multiplexers. (CO2) 6

3.e. Explain the working of serial in serial out (SISO) shift register in detail. (CO3) 6

3.f. Difference between fundamental mode circuits and pulse-mode circuits. (CO4) 6

3.g. Differentiate between SRAM and DRAM. (CO5) 6

SECTION C **50**

4. Answer any <u>one</u> of the following:-

4-a. Implement the original and minimised expression for the function: Y = A' B + AB' + A B using NAND Gate also count the Gate required to implement the boolean expression. (CO1) 10

4-b. Explain the Hamming code. If the Hamming code sequence 1100110 is transmitted and due to error in one position, is received as 1110110, locate the 10

position of the error bit using parity checks and give the method for obtaining the correct sequence. (CO1)

5. Answer any <u>one</u> of the following:-

5-a. Design a combinational circuit that accepts a three-bit number and generate an output. (CO2) 10

5-b. Design a 4 bit magnitude comparator. (CO2) 10

6. Answer any <u>one</u> of the following:-

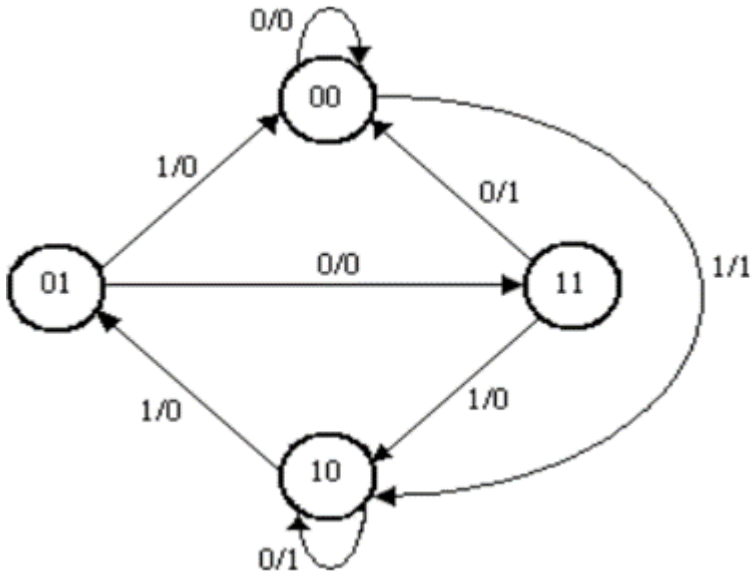
6-a. Explain J-K flip-flop with PRESET and CLEAR inputs using proper logic diagrams and truth tables. (CO3) 10

6-b. Explain the steps involved in the design of sequential logic circuits and Describe the operation of a 2-bit synchronous binary counter. (CO3) 10

7. Answer any <u>one</u> of the following:-

7-a. Enlist the categories of state machines and Draw the state and flow table of asynchronous counter. (CO4) 10

7-b. A sequential Circuit has one input and one output. The state diagram is shown in figure. Design the sequential circuit using D Flip Flop (CO4) 10



8. Answer any <u>one</u> of the following:-

8-a. Compare various programmable devices. (CO5) 10

8-b. Design PAL for a combinational circuit that squares a 3 bit number. (CO5) 10