Printed Page:- Subject Code:- AMTVL0201

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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech.

SEM: II - THEORY EXAMINATION (2021 - 2022)

Subject: Digital Design Using FPGA and CPLD

Time: 3 Hours Max. Marks: 70

General Instructions:

1. The question paper comprises three sections, A, B, and C. You are expected to answer them as directed.
2. Section A - Question No- 1 is 1 marker & Question No- 2 carries 2 marks each.
3. Section B - Question No-3 is based on external choice carrying 4 marks each.
4. Section C - Questions No. 4-8 are within unit choice questions carrying 7 marks each.
5. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION A 15

1. Attempt all parts:-

1 Fault coverage is _____in FSMs. (CO1) 1

(a) Less

(b) More

(c) Equal

(d) None of these

1 The complexity of the asynchronous circuit is involved in timing problems of _____path. (CO2) 1

(a) Input

(b) Output

(c) Feedback Path

(d) Clock Pulses

1 EPROM uses an array of _____. (CO3) 1

(a) p-channel enhancement type MOSFET

(b) n-channel enhancement type MOSFET

(c) p-channel depletion type MOSFET

(d) n-channel depletion type MOSFET

1-d. In FPGA, vertical and horizontal directions are separated by _____. (CO4) 1

(a) line

(b) Channel

(c) Strobe

(d) Flip-Flop

1-e. QFP stand for _____. (CO5) 1

(a) quad flat package

(b) quad fixed package

(c) quad flat processor

(d) None

2. Attempt all parts:-

2.a. Draw the state diagram for JK FF. (CO1) 2

2.b. Define Set-up and Hold Time.(CO2) 2

2.c. Why antifuses are implemented in a PLD? (CO3) 2

2.d. Discuss Pin grid array (PGA) in brief.(CO4) 2

2.e. What is LAB and EAB related to ALTERA FLEX 10K? (CO5) 2

SECTION B 20

3. Answer any five of the following:-

3 Differentiate between Moore model and Mealy model.(CO1) 4

3 Represent Z = (A+BC) with the help of an ASM chart.(CO1) 4

3-c. Differentiate between Static & Dynamic Hazard.(CO2) 4

3-d. A sequential circuit with two D flip-flops A and B, one input x and one output z is specified by the following next-state and output equations: $A(t+1)= A'+B$, $B(t+1)=B'x$, $z=A+B'$ Draw the logic diagram of the circuit.(CO2) 4

3.e. Logic circuits can also be designed using PLDs. Discuss about the given statement.(CO3) 4

3.f. Draw architecture of XILINX XC4000 and discuss it.(CO4) 4

3.g. Describe Macro-Cells with related to Altera MAX 5000 series.(CO5) 4

SECTION C 35

4. Answer any one of the following:-

4-a. Design the circuit for 2 bit Up counter starting from the Moore FSM.(CO1) 7

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|---|---|---|
| 4-b. | Draw the Mealy state diagram and the corresponding ASM chart for the 0101 sequence detector, if repetition is not allowed.(CO1) | 7 |

5. Answer any one of the following:-

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|---|---|---|
| 5-a. | Classify hazards and explain with the help of few examples.(CO2) | 7 |
| 5-b. | Design a synchronous counter using JK-flip flop to count the following sequence 7, 4, 3, 15, 0, 7.(CO2) | 7 |

6. Answer any one of the following:-

| | | |
|---|---|---|
| 6-a. | Why antifuses are implemented in a PLD? Discuss about the other programming techniques.(CO3) | 7 |
| 6-b. | Synthesize the function Z1=AB'+AC' and Z2= A'C+B'C using PLA.(CO3) | 7 |

7. Answer any one of the following:-

| | | |
|---|---|---|
| 7-a. | Discuss in detail FPGA design flow.(CO4) | 7 |
| 7-b. | Write some differences between FPGA and CPLD with diagram.(CO4) | 7 |

8. Answer any one of the following:-

| | | |
|---|---|---|
| 8-a. | Give some difference between Altera series – Max 5000 and Altera series – Max 7000.(CO5) | 7 |
| 8-b. | Design & Implement 7- Segment Display Driver circuit using CPLD.(CO5) | 7 |