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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech.

SEM: II - THEORY EXAMINATION (2021 - 2022)

Subject: Low Power VLSI Design

Time: 3 Hours Max. Marks: 70

General Instructions:

1. The question paper comprises three sections, A, B, and C. You are expected to answer them as directed.
2. Section A - Question No- 1 is 1 marker & Question No- 2 carries 2 marks each.
3. Section B - Question No-3 is based on external choice carrying 4 marks each.
4. Section C - Questions No. 4-8 are within unit choice questions carrying 7 marks each.
5. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION A 15

1. Attempt all parts:-

1 In CMOS logic circuit the n-MOS transistor acts as:(CO1) 1

(a) Load

(b) Pull up network

(c) Pull down network

(d) Not used in CMOS circuits

1-b. Which model is used for scaling?(CO1) 1

(a) constant electric scaling

(b) constant voltage scaling

(c) costant electric and voltage scaling

(d) costant current model

1-c. The flip-flop is only activated by _____(CO3) 1

(a) Positive edge trigger

(b) Negative edge trigger

(c) Either positive or Negative edge trigger

(d) Sinusoidal trigger

1-d. A combinational circuit that selects one from many inputs are _____(CO3) 1

(a) Encoder

(b) Decoder

(c) Demultiplexer

(d) Multiplexer

1-e. The CMOS inverter consists of:(CO1) 1

(a) a) Enhancement mode n-MOS transistor and depletion mode p-MOS transistor

(b) b) Enhancement mode p-MOS transistor and depletion mode n-MOS transistor

(c) c) Enhancement mode p-MOS transistor and enhancement mode p-MOS transistor

(d) d) Enhancement mode p-MOS transistor and enhancement mode n-MOS transistor

2. Attempt all parts:-

2.a. What is the difference between PMOS and NMOS?(CO1) 2

2.b. What is static state power dissipation in CMOS?(CO3) 2

2.c. Explain the Logic Encoding in low power VLSI design?(CO3) 2

2.d. What are the key elements of performance management?(CO4) 2

2.e. What is pre computation logic? Explain.(CO3) 2

SECTION B 20

3. Answer any five of the following:-

3-a. What is leakage current in CMOS? Explain in details with the help of circuit diagram.(CO1) 4

3-b. Explain the flow graph transformation.(CO4) 4

3-c. What is signal entropy?(CO2) 4

3-d. what is monte carlo simulation?(CO2) 4

3.e. Write the difference between combinational and sequential circuits.(CO3) 4

3.f. Explain the power dissipation in clock distribution.(CO5) 4

3.g. what are the steps involved in VLSI design flow?(CO5) 4

SECTION C 35

4. Answer any one of the following:-

4-a. Explain the data correlation analysis in DSP system.(CO2) 7

4-b. Explain the parallel architecture with voltage reduction.(CO4) 7

5. Answer any one of the following:-

5-a. Explain the Probabilistic power analysis technique for low power VLSI circuits.(CO2) 7

5-b.	What are two components of Power dissipation? Explain in detail with circuit diagram.(CO3)	7

6. Answer any one of the following:-

6-a.	Explain the function of S R flip flop. What is the drawback of it?(CO3)	7
6-b.	What is D flip flop? Write the Excitation table and characteristic equation of D flip flop.(CO3)	7

7. Answer any one of the following:-

7-a.	Explain the need for low power VLSI design.(CO4)	7
7-b.	Explain the Low Power Arithmetic Component in details.(CO4)	7

8. Answer any one of the following:-

8-a.	Write short note on zero skew chip Vs tolerable skew chip.(CO5)	7
8-b.	Write short note on single driver Vs distribution buffers.(CO5)	7