Printed Page:- 03 **Subject Code:- AMTVL0201**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: II - THEORY EXAMINATION (2022-2023)

Subject: Digital Design Using FPGA and CPLD

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION A **15**

1. Attempt all parts:-

1-a. Where do/does the status of memory element in a synchronous sequential circuit get/s affected due to change in input? (CO1) 1

(a) At an active edge of clock

(b) At passive edge of clock

(c) Both a and b

(d) None

1-b. One of the properties of Asynchronous circuit is _____. (CO2) 1

(a) Identical mode

(b) Map

(c) Feedback loop

(d) Chart

1-c. To read from the memory, the select input and the power down/program input must be _____. (CO3) 1

(a) HIGH

(b) LOW

(c) Sometimes HIGH and sometimes LOW

(d) Alternate HIGH and LOW

1-d. In FPGA, vertical and horizontal directions are separated by _____. (CO4) 1

(a) A line

(b) Channel

(c) Strobe

(d) Flip-Flop

1-e. The key feature of ispLSI and pLSI 3000 is _____. (CO5) 1

(a) The Premier High Density Families

(b) Unparalleled System Performance

(c) Density with Performance

(d) Cell-Based Logic and Memory

2. Attempt all parts:-

2.a. Draw the state diagram for SR FF. (CO1) 2

2.b. Define primitive flow table. (CO2) 2

2.c. Why antifuses are implemented in a PLD? (CO3) 2

2.d. Name ARM Core Processors which are equipped with Xilinx Zynq™ ZU11EG FPGA. (CO4) 2

2.e. What is ispLSI? (CO5) 2

SECTION B **20**

3. Answer any <u>five</u> of the following:-

3-a. Describe Mealy Model for FSM design with the help of an example. (CO1) 4

3-b. Discuss various types of state machine. (CO1) 4

3-c. Design a binary counter using T flip flops to count in the following sequences: 000, 001, 010, 011, 100, 101, 111, 000. (CO2) 4

3-d. Explain the steps in designing asynchronous sequential circuits. (CO2) 4

3.e. Illustrate the gate level implementation of PLA. (CO3) 4

3.f. What is FPGA? Discuss Taxonomy of FPGA. (CO4) 4

3.g. Elaborate Altera MAX 5000 series Timing Model with diagram. (CO5) 4

SECTION C **35**

4. Answer any <u>one</u> of the following:-

4-a.	Design an FSM (Finite state machine) which will detect three consecutive 1's with overlapping using Mealy Machine. (CO1)	7
4-b.	Given the conditions, such that If A = 1, the circuit oscillates between either one of the two cases. Case 1: 00-01-00-01… and Case 2: 10-11-10-11… And If A = 0, it switches between two cases. Draw the state transition diagram and implement the same using JK flip-flop and by using basic logic gates. (CO1)	7

5. Answer any <u>one</u> of the following:-

5-a.	What do you mean by hazards? Explain Essential hazards and functional hazards in detail. (CO2)	7
5-b.	A synchronous sequential circuit is described by the following excitation and output function Y=X1X2+(X1+X2)Y, Z=Y. (CO2) (i) Draw the logic diagram of the circuit. (ii) Derive the transition table and output map. (iii) Describe the behaviour of the circuit.	7

6. Answer any <u>one</u> of the following:-

6-a.	What is/are the configurable functions of each and every IOBs connected around the FPGA device from the operational point of view? Discuss in detail. (CO3)	7
6-b.	Realization the given functions using PLD: (CO3) F1 = AB'C' + ABC' + ABC F2 = A'BC + AB'C + ABC.	7

7. Answer any <u>one</u> of the following:-

7-a.	Explain 4-bit adder using XC4000 architecture. (CO4)	7
7-b.	Consider the function f (x_1, x_2, x_3) =x_1 (x_2) + x_1x_3 + x_2 x_3 . Show a circuit using 5 two-input lookup-tables (LUTs) to implement this expression. Give the truth table implemented in each LUT. (CO4)	7

8. Answer any <u>one</u> of the following:-

8-a.	Describe Altera series – Max 7000 series architecture and all other aspects in detail. (CO5)	7
8-b.	Design & Implement the Boolean Expression Y=AB+BC+CA on CPLD. (CO5)	7