Printed Page:- 03

Subject Code:- AMTVL0211

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: II - THEORY EXAMINATION (2022-2023)

Subject: VLSI Testing and Testability

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

2022-23 Jan_Jun

SECTION A **15**

1. Attempt all parts:-

1-a. For a circuit with k lines __________ single stuck-at fault is possible. (CO1) 1

(a) k

(b) 2k

(c) k/2

(d) k2

1-b. In D algorithm, a particular ______ fault is detected by examining the ______conditions. (CO2) 1

(a) internal,output

(b) internal,input

(c) external,output

(d) external,input

1-c. In iterative test generation technique, a simple fault in the sequential machine is manifest as __________ multiple faults during test. (CO3) 1

(a) N

(b) N+2

(c) N/2

(d) 2N

1-d. Which method is more accurate? (CO4) 1

(a) Pseudo-random testing

(b) Random testing

(c) LFSR

(d) Cellular automata

1-e. Signature analysis performs (CO5) 1

(a) addition

(b) multiplication

(c) polynomial divison

(d) amplifies

2. Attempt all parts:-

2.a.	What are the differences between DC and AC parametric test?	2
2.b.	What do you mean by consistency?	2
2.c.	Write the sequential ATPG approach.	2
2.d.	Define delay faults.	2
2.e.	What is BILBO?	2

SECTION B **20**

3. Answer any five of the following:-

3-a.	What is the total number of single stuck-at faults, counting both stuck-at-0 and stuck-at-1, if the number of primary inputs is 2, total number of gate is 2 and number of fan out branches is 2? (CO1)	4
3-b.	Explain the various problems associated with ideal test.(CO1)	4
3-c.	Write all the steps of a D algorithm.(CO2)	4
3-d.	Discuss the advantages of removal of redundant hardware.(CO2)	4
3.e.	What are the things that should be followed by partial scan method? (CO3)	4
3.f.	Explain the different factors on which the switching delay depends. (CO4)	4
3.g.	Write and briefly explain the four different modes of BILBO operation.(CO5)	4

SECTION C **35**

4. Answer any one of the following:-

2022-23 Jan_Jun

4-a.	Explain in detail the external representation and internal representation in structural models of VLSI circuits.(CO1)	7
4-b.	What is fault model? What are the characteristics of a good fault model? Why stuck at- fault model is widely accepted? (CO1)	7

5. Answer any <u>one</u> of the following:-

5-a.	Discuss the Test Generation Methods and explain Boolean difference method. (CO2)	7
5-b.	Explain Pernicious Fault Masking with suitable example. (CO2)	7

6. Answer any <u>one</u> of the following:-

6-a.	How can the flip flops themselves be tested in scan chain based testing? Explain in detail. (CO3)	7
6-b.	With the help of a neat sketch explain the logic of a boundary scan test. (CO3)	7

7. Answer any <u>one</u> of the following:-

7-a.	Explain any suitable design parameters for IDDQ testability patterns. (CO4)	7
7-b.	Discuss the test algorithms for RAM with their advantages and disadvantages. (CO4)	7

8. Answer any <u>one</u> of the following:-

8-a.	What is Built-In-Self-Test? Discuss the issues and benefits of BIST. Describe BIST architecture and its operation. (CO5)	7
8-b.	Discuss the features of Pseudo-random testing and Pseudo-exhaustive testing with suitable example. (CO5)	7

2022-23 Jan_Jun