Printed Page:- 03 **Subject Code:- AMTVL0202**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: II - THEORY EXAMINATION (2023 - 2024)

Subject: Low Power VLSI Design

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION A **15**

1. Attempt all parts:-

1-a. VLSI technology uses _____ to form integrated circuit. (CO1) 1

(a) transistors

(b) switches

(c) diodes

(d) buffers

1-b. Simulator converts circuit information to (CO2) 1

(a) design plan

(b) does verification

(c) set of equations

(d) floor plan

1-c. How many stable states combinational circuits have? (CO3) 1

(a) 3

(b) 4

(c) 2

(d) 5

1-d. Power dissipation in switch logic is (CO4) 1

(a) less

(b) more

(c) high

(d) very less

1-e. In negative logic convention, the Boolean Logic [1] is equivalent to: (CO5) 1

(a) +VDD

(b) 0 V

(c) -VDD

(d) None of the mentioned

2. Attempt all parts:-

2.a. What is W/ L ratio? (CO1) 2

2.b. What is static power dissipation in CMOS? (CO2) 2

2.c. What is Gray Code? (CO3) 2

2.d. What is the basis of power consumption in VLSI circuit? (CO4) 2

2.e. How the propogation delay get affected by increasing fanout? (CO5) 2

SECTION B **20**

3. Answer any <u>five</u> of the following:-

3-a. Draw the fabrication steps of NMOS transistor and explain its operation in detail. (CO1) 4

3-b. Why PMOS transistor size is double the size of NMOS transistor? (CO1) 4

3-c. Write short notes on gate oxide thickness. (CO2) 4

3-d. Explain Threshold voltage in CMOS, write it's importance. (CO2) 4

3.e. Write the Excitation table and characteristic equation of T flip flop. (CO3) 4

3.f. What are the objectives of performance management? (CO4) 4

3.g. What is multiplexer? Explain with the help of circuit diagram. (CO5) 4

SECTION C **35**

4. Answer any <u>one</u> of the following:-

4-a. Explain parasitic capacitance with the help of diagram. (CO1) 7

4-b. How can leakage current be reduced in CMOS? Explain with circuit diagram. (CO1) 7

5. Answer any <u>one</u> of the following:-

5-a.	Explain probabilistic power estimation approaches. (CO2)	7
5-b.	What are the 5 steps of a simulation? Explain in detail. (CO2)	7

6. Answer any <u>one</u> of the following:-

6-a.	Explain briefly the difference between the Mealy model and Moore model. (CO3)	7
6-b.	What are the differences between synchronous and asynchronous counter? (CO3)	7

7. Answer any <u>one</u> of the following:-

7-a.	What is Flow Graph Transformation? Explain in details. (CO4)	7
7-b.	What is adaptive performance management? Explain. (CO4)	7

8. Answer any <u>one</u> of the following:-

8-a.	What is CMOS? Implement CMOS circuit of given boolean expression Y=(ab+c+d)'. (CO5)	7
8-b.	What do you mean by Package Co-design of clock network? Explain. (CO5)	7