Printed Page:- 03 **Subject Code:- AMTVL0211**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: II - THEORY EXAMINATION (2023 - 2024)

Subject: VLSI Testing and Testability

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

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SECTION A **15**

1. Attempt all parts:-

1-a. Input to a testing process (CO1) 1

(a) Test stimuli

(b) Circuit under test

(c) Both test stimuli and circuit under test

(d) None of these

1-b. The efficiency of the test pattern generation is improved by (CO2) 1

(a) adding buffers

(b) adding multipliers

(c) partitioning

(d) adding power dividers

1-c. The boundary scan path tests the (CO3) 1

(a) input nodes

(b) output nodes

(c) input and output nodes

(d) interconnection points

1-d. IDDQ fault occurs when there is (CO4) 1

(a) increased voltage

(b) increased quiescent current

(c) increased power supply

(d) increased discharge

1-e. _____ gate is used to ensure whether the test patterns have sufficient clock cycles. (CO5) 1

(a) NOT

(b) NAND

(c) AND

(d) None of These

2. Attempt all parts:-

2.a. Write the different challenges in VLSI testing. (CO1) 2

2.b. What do you mean by D- Intersection? (CO2) 2

2.c. Why Sequential ATPG are not widely used in industry? (CO3) 2

2.d. What is coupling fault?(CO4) 2

2.e. What are the features of a test data compression?(CO5) 2

SECTION B **20**

3. Answer any <u>five</u> of the following:-

3-a. Explain about on multiple stuck-fault models.(CO1) 4

3-b. Why some additional circuitry (design for testability) is required in structural testing?(CO1) 4

3-c. What do you mean by propagation D cube? Explain with example.(CO2) 4

3-d. Discuss the difference between D algorithm and PODEM algorithm. (CO2) 4

3.e. What are the things that should be avoided in ad-hoc DFT methods?(CO3) 4

3.f. Write the name of different fault models of static RAM.(CO4) 4

3.g. With the help of good example discuss the differences between pseudo exhaustive test generation and pseudo random test generation methods.(CO5) 4

SECTION C **35**

4. Answer any <u>one</u> of the following:-

4-a. What is meant by fault collapsing? Explain the importance of fault collapsing.(CO1) 7

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4-b.	What is fault model? What are the characteristics of a good fault model? Why stuck at- fault model is widely accepted? (CO1)	7

5. Answer any <u>one</u> of the following:-

5-a.	Discuss the Test Generation Methods and explain Boolean difference method. (CO2)	7
5-b.	Discuss the complexity of D – algorithm with suitable example.(CO2)	7

6. Answer any <u>one</u> of the following:-

6-a.	Explain the partial scan design method of a combinational circuit with suitable example.(CO3)	7
6-b.	Discuss the differences between ad-hoc design technique and scan path technique.(CO3)	7

7. Answer any <u>one</u> of the following:-

7-a.	Describe the different faults that can be detected by IDDQ testing with suitable diagram (CO4)	7
7-b.	What do you mean by IDDQ testing? Explain the principle of IDDQ testing.(CO4)	7

8. Answer any <u>one</u> of the following:-

8-a.	With the help of neat diagram explain BIST architectures of LOCST and RTD. (CO5)	7
8-b.	What is pseudo-random pattern generation? What is an LFSR? Describe pattern generation using LFSR.(CO5)	7

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