Printed Page:-

Roll No

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute)

Affiliated to Dr. A.P.J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow

M.TECH

FIRST YEAR (SEMESTER-II) THEORY EXAMINATION (2020-2021)

Subject Code: AMTVL0201

Subject: I Subject: Digital Design Using FPGA and CPLD

Max. Mks. : 40

Time : 70 Minutes

General Instructions:

All questions are compulsory.

Question No- 1 to 5 are objective type question carrying 2 marks each.

Question No- 6 to 20 are also objective type/Glossary based question carrying 2 marks each.

Q.No	Question Content	Question Image	Category	Sub Category	Marks	Options Randomization	Type	Difficulty	Correct	Option1	Option2	Option3	Option4
1	What happens when input is high in FSM?		Single Choice Questions	Single Choice Questions	2		Single Choice	Brilliant	Change of state	Change of state	No transition in state	Remains in a single state	Invalid state
2	The race in which stable state depends on an order is called _____.		Single Choice Questions	Single Choice Questions	2		Single Choice	Brilliant	Critical race	Critical race	Non-Critical race	identical race	defined race
3	What is the difference between static RAM and dynamic RAM?		Single Choice Questions	Single Choice Questions	2		Single Choice	Smart	Dynamic RAM must be refreshed, static RAM does not	Static RAM must be refreshed, dynamic RAM does not	There is no difference	Dynamic RAM must be refreshed, static RAM does not	SRAM is slower than DRAM
4	In FPGA, vertical and horizontal directions are separated by _____.		Single Choice Questions	Single Choice Questions	2		Single Choice	Brilliant	Channel	line	Channel	Strobe	Flip-Flop
5	_____expanders are inverted product terms that are fed back into the logic array.		Single Choice Questions	Single Choice Questions	2		Single Choice	Brilliant	Shareable	Parallel	Shareable	both Parallel and Shareable	none of the above
6	The NOR function is the dual of _____function.		Glossary I	Glossary I	2		Single Choice	Brilliant	NAND	NAND	Change of state	Two	
7	The SR latch consist of_____inputs.		Glossary I	Glossary I	2		Single Choice	Brilliant	Two	NAND	Change of state	Two	
8	In FSM diagram what does arrow between the circles represent_____		Glossary I	Glossary I	2		Single Choice	Brilliant	Change of state	NAND	Change of state	Two	
9	State table can be represented in a_____		Glossary II	Glossary II	2		Single Choice	Brilliant	State diagram	Feedback loop	D	State diagram	
10	_____flip-flop is used to provide delay.		Glossary II	Glossary II	2		Single Choice	Brilliant	D	Feedback loop	D	State diagram	
11	One of the properties of Asynchronous circuit is_____		Glossary II	Glossary II	2		Single Choice	Brilliant	Feedback loop	Feedback loop	D	State diagram	
12	SPLDs, CPLDs, and FPGAs are all_____type of device.		Glossary III	Glossary III	2		Single Choice	Brilliant	PLD	LUT	after the programmable AND arrays	PLD	
13	_____is commonly found in FPGAs.		Glossary III	Glossary III	2		Single Choice	Brilliant	LUT	LUT	after the programmable AND arrays	PLD	
14	The macrocells in a PAL are located_____.		Glossary III	Glossary III	2		Single Choice	Brilliant	after the programmable AND arrays	LUT	after the programmable AND arrays	PLD	
15	_____are used to connect adjacent blocks.		Glossary IV	Glossary IV	2		Single Choice	Brilliant	Single Length lines	Long lines	Global lines	Single Length lines	

Q.No	Question Content	Question Image	Category	Sub Category	Marks	Options Randomization	Type	Difficulty	Correct	Option1	Option2	Option3	Option4
16	_____is used for power, ground and clock signals.		Glossary IV	Glossary IV	2		Single Choice	Brilliant	Global lines	Long lines	Global lines	Single Length lines	
17	_____are distributed over long distances.		Glossary IV	Glossary IV	2		Single Choice	Brilliant	Long lines	Long lines	Global lines	Single Length lines	
18	_____ increases the number of product terms by borrowing unused product from other macrocells.		Glossary V	Glossary V	2		Single Choice	Brilliant	Parallel expander	EEPROM	an OR-gate array and some output logic	Parallel expander	
19	The Altera MAX 7000 series uses _____ process technology.		Glossary V	Glossary V	2		Single Choice	Brilliant	EEPROM	EEPROM	an OR-gate array and some output logic	Parallel expander	
20	A macrocell basically contains _____.		Glossary V	Glossary V	2		Single Choice	Brilliant	an OR-gate array and some output logic	EEPROM	an OR-gate array and some output logic	Parallel expander	