Printed Page:- Subject Code:- AEC0301

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech.

SEM: III - THEORY EXAMINATION (2021 - 2022)

Subject: Digital System Design

Time: 03:00 Hours Max. Marks: 100

General Instructions:

1. All questions are compulsory. It comprises of three Sections A, B and C.

- Section A - Question No- 1 is objective type question carrying 1 mark each & Question No- 2 is very short type questions carrying 2 marks each.
- Section B - Question No- 3 is Long answer type - I questions carrying 6 marks each.
- Section C - Question No- 4 to 8 are Long answer type - II questions carrying 10 marks each.
- No sheet should be left blank. Any written material after a Blank sheet will not be evaluated/checked.

SECTION A 20

1. Attempt all parts:-

1-a. Hamming code is capable of (CO1) 1

1. Only detect single-bit error
2. Only correct single-bit error
3. Detect and correct single bit error
4. Detect and correct multiple bit errors

1-b. Find the 2’s complement of 1101011101000. (CO1) 1

1. 1101011101000
2. 1001011101000
3. 1011101001
4. None of these

1-c. In four-variable K-map simplification, a group of eight adjacent ones leads to a term with (CO2) 1

1. one literal
2. two literal
3. three literal
4. four literal

1-d. What is a multiplexer? (CO2) 1

1. It is a type of decoder which decodes several inputs and gives one output
2. A multiplexer is a device which converts many signals into one
3. It takes one input and results into many output
4. It is a type of encoder which decodes several inputs and gives one output

1-e. When both inputs of SR latches are high, the latch goes _____. (CO3) 1

1. Unstable
2. Stable
3. Indeterminate state
4. Bistable

1-f. What is a trigger pulse? (CO3) 1

1. A pulse that starts a cycle of operation
2. A pulse that reverses the cycle of operation
3. A pulse that prevents a cycle of operation
4. A pulse that enhances a cycle of operation

1-g. The basic function of TTL gate is which of the following functions? (CO4) 1

1. AND
2. OR
3. NOR
4. NAND

1-h. If a logic circuit has fanout of 4, then the circuit is (CO4) 1

1. 4 input
2. has 4 outputs
3. can derive maximum of 4 outputs
4. Gives output 4 times the input

1-i. For 5K memory, how many address lines are needed? (CO5) 1

1. 10
2. 13
3. 12
4. 9

1-j. Which one is volatile? (CO5) 1

1. DROM
2. Secondary Memory
3. RAM
4. Random only memory

2. Attempt all parts:-

2-a. Draw the logical circuit of AND Gate using NOR Gate. (CO1) 2

2-b. Minimise the following function in SOP minimal form using K- Maps: f(A,B,C,D) = m(1, 5, 6, 12, 13, 14) + d(4). (CO2) 2

2-c. Write the truth table of JK Flip-Flop. (CO3) 2

2-d. State the advantages of ECL family. (CO4) 2

2-e. Differentiate between PAL and PLA. (CO5) 2

SECTION B 30

3. Answer any <u>five</u> of the following:-

3-a.	Construct the Hamming code for the 4 bit data 1010. Consider the even parity. (CO1)	6
3-b.	Convert the following decimal numbers to the indicated bases: (a) 7562.45 to octal. (b) 1938.257 to hexadecimal. (c) 175.175 to binary. (CO1)	6
3-c.	Implement the SUM and CARRY Boolean functions of full adder with multiplexers. (CO2)	6
3-d.	Explain one digit BCD Adder using 7483 ICs. (CO2)	6
3-e.	Draw JK flip-flop and derive its characteristic equation. Explain how will you convert it into T flip-flop. (CO3)	6
3-f.	Draw the circuit diagram of CMOS NOT gate and explain its working. (CO4)	6
3-g.	Implement the following functions using PAL. F1 (A,B,C)= $\sum(3,5,6,7)$ and F2 (A,B,C)= $\sum(0,2,4,7)$. (CO5)	6

SECTION C 50

4. Answer any one of the following:-

4-a.	Realize the XOR and XNOR logic operation using NAND gate. (CO1)	10
4-b.	Find the complement of the following expressions: (a) xy' + x'y (b) (AB' + C)D' + E (c) AB(C'D + CD') + A'B'(C' + D)(C + D') (d) (x + y' + z)(x' + z')(x + y) (CO1)	10

5. Answer any one of the following:-

5-a.	Design a combinational circuit that will compare two 4-bit numbers. (CO2)	10
5-b.	Minimize the given function by QM method. F(A,B,C,D) = $\sum m(0,1,2,3,10,11,12,13,14,15)$. (CO2)	10

6. Answer any one of the following:-

6-a.	Design a synchronous Mod-10 counter using D or T flip-flops. (CO3)	10
6-b.	Explain universal shift register in detail. (CO3)	10

7. Answer any one of the following:-

7-a.	Explain the following with respect to logic families: Fanout, Fan-In, Propagation delay and noise margin. (CO4)	10
7-b.	Explain Totem pole output connection of TTL logic family along with its applications? (CO4)	10

8. Answer any one of the following:-

8-a.	Classify semiconductor Memories and explain Erasable PROM in detail. (CO5)	10
8-b.	Realize the given functions using PLD: F1 = AB'C' + ABC' + ABC and F2 = A'BC + AB'C + ABC. (CO5)	10